An All-Digital Jitter Tolerance Measurement Technique for CDR Circuits

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***Abstract*—An all-digital on-chip jitter tolerance measurement technique for clock/data recovery (CDR) circuits is presented. A 6-Gbps CDR circuit with this proposed technique is realized in a 90-nm CMOS process. The measured jitter tolerance by using the testing equipment and the proposed technique correlate within 13% in the frequency range of 178 kHz $\sim$ 11.3 MHz. The measured peak-to-peak data and clock jitters are 15.56 and 13.3 ps. The power of the CDR circuit is 44.4 mW at a supply voltage of 1.2 V.**

***Index Terms*—All-digital, clock and data recovery, jitter tolerance.**

I. Introduction

TO ENSURE the signal integrity for high-speed data transmission, clock/data recovery (CDR) circuits must tolerate the input data with substantial jitters, which are induced by power noise, frequency mismatch, device noises, and so on. The jitter tolerance [1]–[6] is used to gauge a CDR circuit, that how much input data jitter it could tolerate while the bit-error-rate (BER) is still lower than a target value. Usually, it needs the automatic test equipment to measure the CDR circuits for mass production. To reduce the cost, it is indispensable to realize an on-chip approach to measure the jitter tolerance of a CDR circuit. In [6], an analog approach is presented by using a digital-to-analog converter and a modulating charge pump. This approach superimposes a sine wave onto the control voltage of a voltage-controlled oscillator (VCO) to modulate the clock instead of the data. Since the exact values of each component are unknown, the calibration has to be done before each measurement [6].

In this brief, an all-digital jitter tolerance measurement technique for CDR circuits is presented. An all-digital jitter modulation is applied to a pseudo-random binary sequence (PRBS) data by modulating a divide-by-$N/N+1$ dual-modulus prescaler. It measures the on-chip jitter tolerance of a CDR circuit without external jitter tolerance testing equipment. This technique reduces the testing cost, and it can be applied to various analog/digital CDR circuits. In addition, this all-digital technique relaxes the sensitivity of analog circuits to the process variations and noises in the testing environment.

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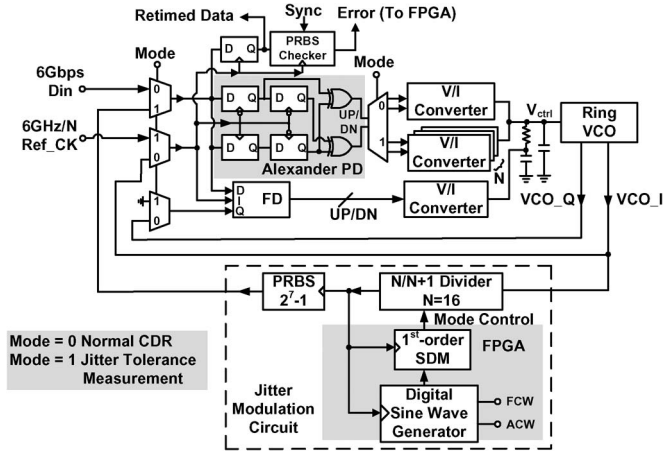

Fig. 1. Proposed CDR circuit with an on-chip jitter tolerance measurement.

II. System Description

A CDR circuit using the on-chip jitter tolerance measurement is shown in Fig. 1. It consists of a conventional CDR circuit and a jitter modulation circuit. This CDR circuit is realized by the Alexander phase detector (PD) [7], a frequency detector (FD) [8], voltage-to-current (V/I) converters, a passive loop filter, a four-stage ring VCO, a PRBS checker, and the multiplexers. The jitter modulation circuit consists of a divide-by-$N/N+1$ dual-modulus prescaler, where $N=16$; a PRBS of 2^7-1; a first-order sigma–delta modulator (SDM); and a digital sine wave generator. When Mode $=0$, the multiplexers connect the input data of 6 Gbps and the VCO's quadrature outputs, namely, VCO-I and VCO-Q, to the PD and FD. Fig. 1 operates as a conventional CDR circuit. When Mode $=1$, the multiplexers switch a PRBS of 2^7-1 and the reference clock, Ref_CK, of 6/N-GHz to the PD. Since the data rate of this PRBS is lowered N times, the loop gain of this CDR circuit is also lowered by N times. To keep the loop gain of this CDR circuit constant, the V/I converter is scaled by N times. This VCO still operates at 6 GHz in this work. A digital sine wave generator and a first-order SDM modulate the division ratio of the divide-by-$N/N+1$ dual-modulus prescaler. The VCO is divided by a divide-by-$N/N+1$ dual-modulus prescaler. This divided clock acts as a clock of the PRBS, so that a sine wave jitter is digitally modulated into a PRBS. Therefore, the BER of this CDR circuit is measured by using a PRBS checker. The amplitude and frequency of this digital sine wave generator are digitally adjusted by the amplitude control word (ACW) and frequency control word (FCW), respectively. As a result, the relation between the BER and the jitter modulation amplitude/frequency can be digitally obtained. In this brief, since the sine wave is periodic, the bit stream outputs of the digital sine wave generator and

the first-order SDM are calculated first. Then, these bit stream outputs are stored in the memory of a field-programmable gate array (FPGA). However, the operation frequency of 6/N-GHz is still too high for our FPGA. The parallel 8-bits interface is adopted to reduce the operation frequency between this chip and the FPGA. To control the dual-modulus prescaler, an on-chip parallel-to-series converter is realized in this work. If the digital circuits or the memory can operate at higher than 375 MHz, this FPGA can be replaced.

III. Performance Analysis

A. Jitter Modulation Generation

The sine wave is digitized by a first-order SDM into a bit stream to modulate the divide-by-$N/N+1$ dual-modulus prescaler. The output frequency of the divide-by-$N/N+1$ dual-modulus prescaler is expressed as

$$\omega_{\text{divider}} = \frac{\omega_{\text{out}}}{N + f(\omega_m)} \tag{1}$$

where $f(\omega_m) = 0.5 + N_A \sin(\omega_m)$, $0 \le N_A \le 0.5$, and $N = 16$. ω_m and N_A are the frequency and amplitude of this sine wave, respectively. ω_{out} is the output frequency of the VCO. When $N_A/N \ll 1$ and the frequency of the sine wave generator is equal to ω_m, the output frequency of the dual-modulus prescaler is approximated as

$$\begin{aligned}\omega_{\text{divider}} &= \frac{\omega_{\text{out}}}{N + 0.5 + N_A \sin(\omega_m t)} \\ &\cong \frac{\omega_{\text{out}}}{N+0.5}\left(1 - \frac{N_A \sin(\omega_m t)}{N+0.5}\right).\end{aligned} \tag{2}$$

To integrate ω_{divider}, the corresponding phase is given as

$$\begin{aligned}\phi_{\text{divider}} &= \int \omega_{\text{divider}} dt \\ &= \frac{\omega_{\text{out}} t}{N+0.5} + \frac{\omega_{\text{out}} N_A}{\omega_m (N+0.5)^2}\cos(\omega_m t).\end{aligned} \tag{3}$$

According to (3), the phase amplitude and angular frequency of this sinusoidal modulation jitter are equal to $\omega_{\text{out}} N_A/\omega_m(N+0.5)^2$ and ω_m, respectively. Note that the phase amplitude is digitally adjusted by ω_m and N_A of the digital sine wave generator. Thus, it can measure the jitter tolerance performance of a CDR circuit. Moreover, no additional calibration is needed compared with [6]. The ramp term of $\omega_{\text{out}} t/(N+0.5)$ in (3) is equivalent to a constant frequency, and the CDR circuit will track it.

B. Jitter Tolerance Analysis

The bang-bang CDR jitter tolerance has been studied in [9]. When input jitter is expressed as

$$\phi_{\text{in}}(t) = \phi_{\text{in},p} \cos(\omega_\phi \cdot t) \tag{4}$$

the maximum phase error $\Delta\phi_{\max}$ is derived as

$$\Delta\phi_{\max} = \frac{\sqrt{4\omega_\phi^2 \phi_{\text{in},p}^2 - \pi^2 K_{\text{VCO}}^2 I_p^2 R_p^2}}{2\omega_\phi} \tag{5}$$

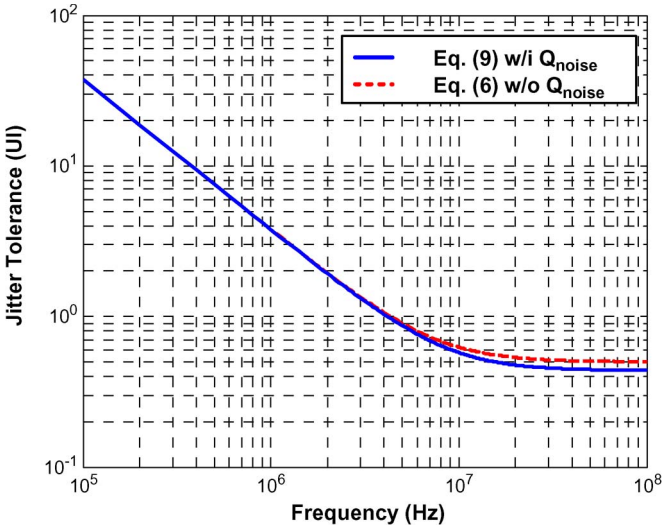

Fig. 2. Simulated jitter tolerance by (solid line) (6) and (dash line) (9).

where K_{VCO} is the VCO's gain, I_p is the current of the V/I converter, and R_p is the resistance of the loop filter. While $\Delta\phi_{\max} = \pi$, the maximum input tolerable jitter is given as

$$\phi_{\text{in},p} = G_{\text{JT}} = \pi\sqrt{1 + \frac{K_{\text{VCO}}^2 I_p^2 R_p^2}{4\omega_\phi^2}}. \tag{6}$$

In our case, the SDM may induce the quantization noise, which deteriorates the maximum input tolerable jitter. The maximum induced quantization noise is

$$Q_{\text{noise}} = \frac{2\pi}{N}. \tag{7}$$

Consider a worse case, the maximum phase error becomes

$$\Delta\phi_{\max} = \pi - \frac{2\pi}{N}. \tag{8}$$

Similarly, by (5), the jitter tolerance with a quantization noise is given as

$$G_{\text{JT,Qnoise}} = \pi\sqrt{\left(\frac{N-2}{N}\right)^2 + \frac{K_{\text{VCO}}^2 I_p^2 R_p^2}{4\omega_\phi^2}}. \tag{9}$$

The simulated jitter tolerances of (6) and (9) are shown in Fig. 2, where $K_{\text{VCO}} = 2\pi(2 \cdot 10^9)$ rad/V, $R_p = 150$ ohm, $N = 16$, and $I_p = 50$ μA. From Fig. 2, when $\omega_\phi \gg K_{\text{VCO}} I_p R_p/2$, the second term within the square root of (9) and (6) can be negligible. The jitter tolerance approaches a constant when the jitter frequency is large. By the proposed technique, the quantization noise slightly degrades the jitter tolerance when the jitter frequency is higher than the bandwidth of the CDR circuit.

C. Upper Bound of Modulation Jitter

From the second term in (3), when $N_{\text{A}} = 0.5$, the maximum phase amplitude of this sinusoidal modulation jitter is

$$\frac{\omega_{\text{out}}}{2\omega_m(N+0.5)^2} \tag{10}$$

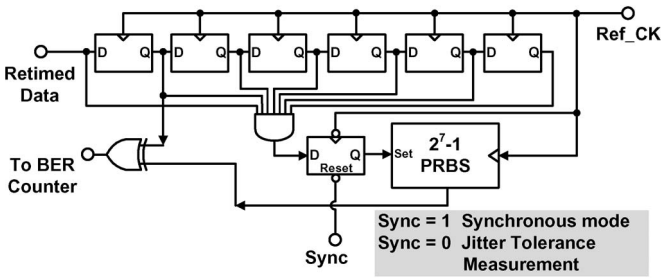

Fig. 3. PRBS checker.

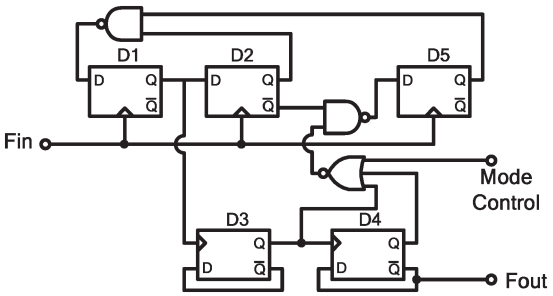

Fig. 4. Divide-by-16/17 dual-modulus prescaler.

where ω_{out} is the output frequency of a CDR circuit, and ω_m is the input jitter frequency. These two parameters are predefined and cannot be easily changed. Thus, N is the only one parameter that can be altered. To choose an adequate value of N, the following considerations are discussed. First, from (7) and (9), the effect caused by the quantization noise is negligible while N is as large as possible. Second, from (9), the upper bound of the jitter tolerance is inversely proportional to N, which should cover a sufficient jitter tolerance range. Third, the speed of an FPGA is limited by the minimum value of N. In order to have a sufficient timing budget for digital circuits, a large N is preferred. Based on the above considerations, to satisfy the jitter tolerance range, the FPGA timing budget, and the low quantization noise, $N = 16$ is chosen in this work.

IV. Circuit Description

A. PRBS Checker

The PRBS checker is shown in Fig. 3. It has to synchronize with the PRBS of $2^7 - 1$ connected to the divide-by-$N/N + 1$ dual-modulus prescaler before the jitter tolerance is measured. When the signal "Sync" is set to high, a seven-input AND gate and six D-flip-flops (DFFs) are used to detect the pattern of "1111111" and synchronize them. When the signal "Sync" is set to low, the BER is calculated by comparing the retimed data of the CDR circuit and the PRBS checker by a XOR gate.

B. Divide-by-16/17 Dual-Modulus Prescaler

A divide-by-16/17 dual-modulus prescaler is shown in Fig. 4. When the signal "Mode Control" is high, the DFFs, namely, D1, D2, and D5, realize a divide-by-4 operation. The following DFFs, namely, D3 and D4, realize a divide-by-16 output. When the signal "Mode Control" goes low, the DFF D5 will be activated to swallow one clock. A divide-by-17 operation will be realized.

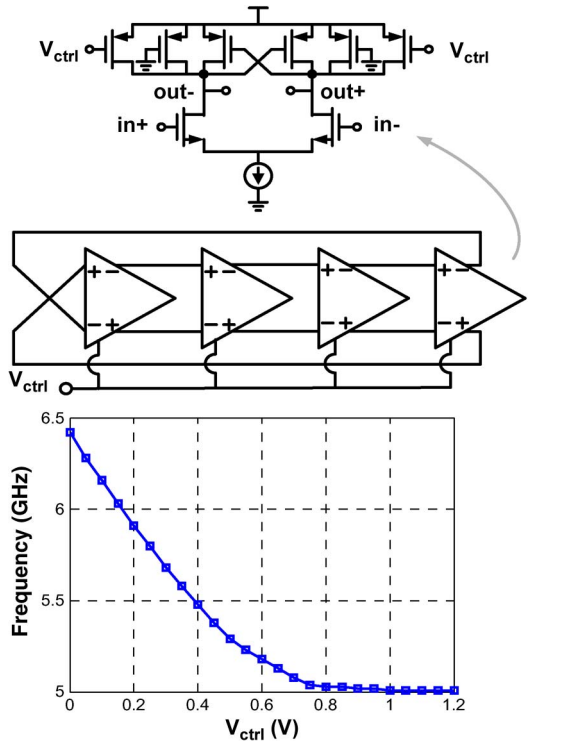

Fig. 5. (a) Four-stage VCO and its delay stage. (b) Measured transfer curve of the VCO.

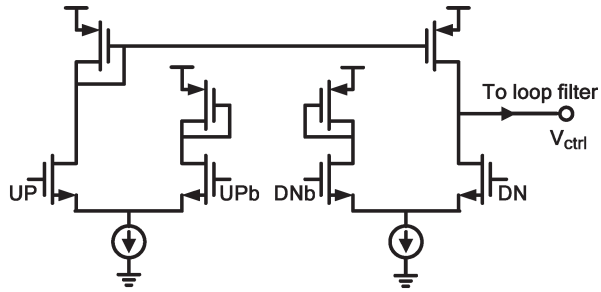

Fig. 6. V/I converter.

C. Four-Stage Ring VCO

The VCO is realized by a four-stage ring oscillator. The delay stage is a differential pair with the cross-coupled load and voltage-controlled resistors, as shown in Fig. 5(a). The measured transfer curve is shown in Fig. 5(b). The VCO tuning range is from 5.01 to 6.42 GHz.

D. V/I Converter

The V/I converter is implemented by two differential pairs with active loads, as shown in Fig. 6. Since the tail current sources are always active, it reduces the switching noises on power supply. The tail current source is chosen as 50 μA.

V. Experimental Results

A. Measurement Setup

The measurement setup by the off-the-shelf equipment and the proposed technique are shown in Fig. 7(a) and (b),

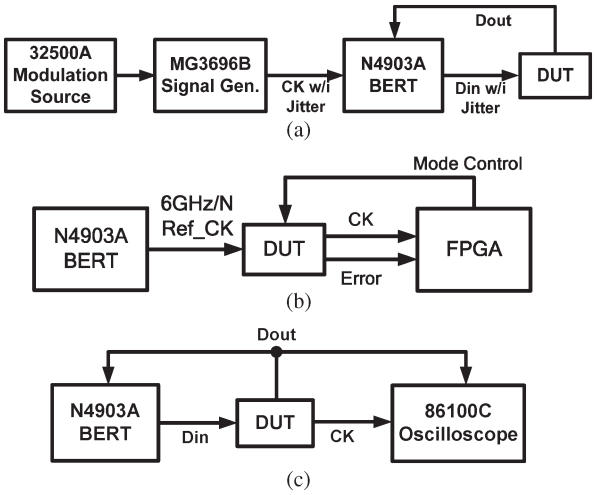

Fig. 7. Jitter tolerance measurement by the (a) off-the-shelf equipment and the (b) proposed technique; (c) jitter and eye diagram measurements.

respectively. Fig. 7(a) measures the jitter tolerance of the CDR circuit by using the off-the-shelf equipment. The clock with sinusoidal modulation jitters is generated by a modulation source 33250A and a signal generator MG3696B. The clock with jitters then applies to N4903A to generate the data with jitters to test the jitter tolerance of a CDR circuit. The recovered data is feedback to the N4903A BERT module to calculate the BER.

Fig. 7(b) measures the jitter tolerance by the proposed technique. In this measurement, a reference clock is applied to the CDR circuit rather than data. The divided clock and the signal "Error" of the CDR circuit are applied to the FPGA. This signal "Error" comes from the PRBS checker, and it is sent to the FPGA for calculating the BER. Fig. 7(c) shows the setup to measure the jitter of the recovered clock and the eye diagram of the CDR circuit.

B. Measurement Results

The jitter tolerance measurements by the proposed technique are shown in Fig. 8(a). The symbols "o" and "x" represent the measurement results that are less and larger than a BER of 10^{-9}, respectively. The boldface dash line represents the upper bound of the frequency and amplitude of the sinusoidal modulation jitter. The frequency and amplitude of the sinusoidal modulation jitter are controlled by FCW and ACW in the digital sine wave generator, respectively. The modulation frequency ranges from 178 kHz to 11.3 MHz. The lowest frequency is limited by the memory size of the FPGA, and the highest one is limited by the upper bound for the modulation amplitude. The upper bound for the modulation amplitude in a specified frequency is determined by (10). Fig. 8(b) shows the measured jitter tolerances by using the off-the-shelf equipment and the proposed technique, which correlate within 13% in the measured frequency range of 178 kHz $\sim$ 11.3 MHz. To improve the measured root-mean-square (rms) error, the quantization noise of the SDM should be reduced, and the division ratio of N should be increased. However, it may reduce the jitter modulation range according to (10).

Fig. 9(a) and (b) shows the measured eye diagram and the recovered clock of this 6-Gbps CDR circuit for a PRBS of $2^7 - 1$, respectively. The measured peak-to-peak jitters of the

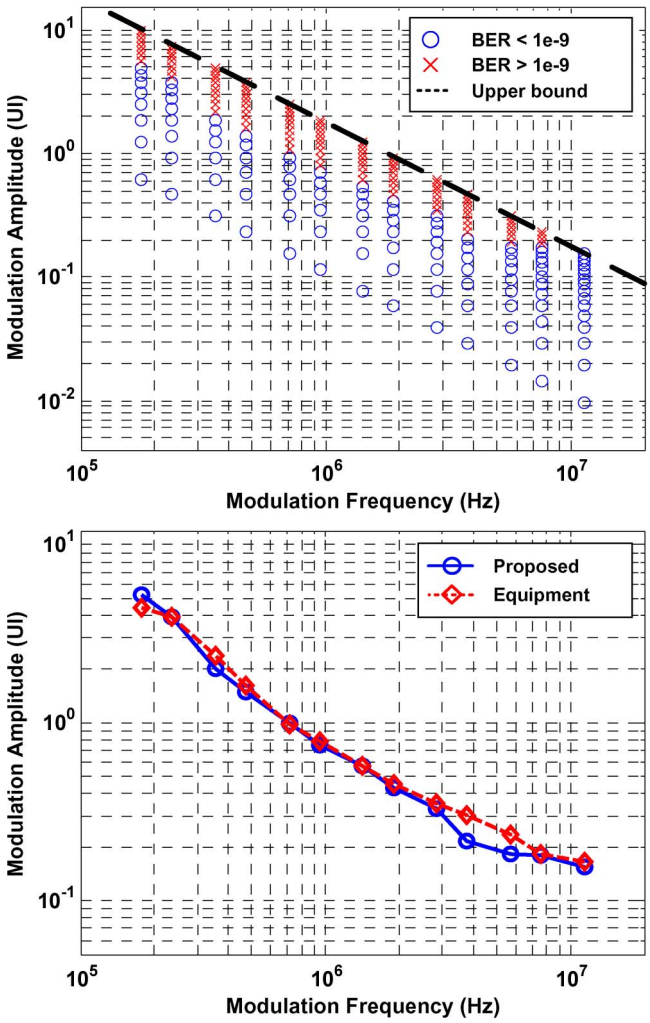

Fig. 8. (a) Jitter tolerance measurements by the proposed technique. (b) Measured jitter tolerances using the off-the-shelf equipment and the proposed technique.

recovered data and clock are 15.56 and 13.3 ps, respectively. The measured rms jitters of the recovered data and clock are 2.2 and 1.68 ps, respectively.

The die photo of this work is shown in Fig. 10. It is realized in a 90-nm CMOS process. The power consumption of the CDR circuit is 44.4 mW for a supply voltage of 1.2 V. The area of this CDR circuit is 0.054 mm^2. Note that an 8-bits parallel-to-serial circuit is used to relax the bandwidth requirement between the FPGA and this chip. Table I shows the performance summary and comparison among this work and [2] and [6]. By using this proposed technique, the jitter tolerance of a CDR circuit can be measured on a chip without external jitter tolerance testing equipment. Due to its digital feature, no calibration is needed for the jitter tolerance measurement compared with [6]. This technique can be applied to various analog/digital CDR circuits.

VI. Conclusion

An all-digital on-chip jitter tolerance measurement technique for CDR circuits is presented. The proposed circuit is realized by a 90-nm CMOS process. The theoretical analysis and measured results are given to demonstrate this technique. By using

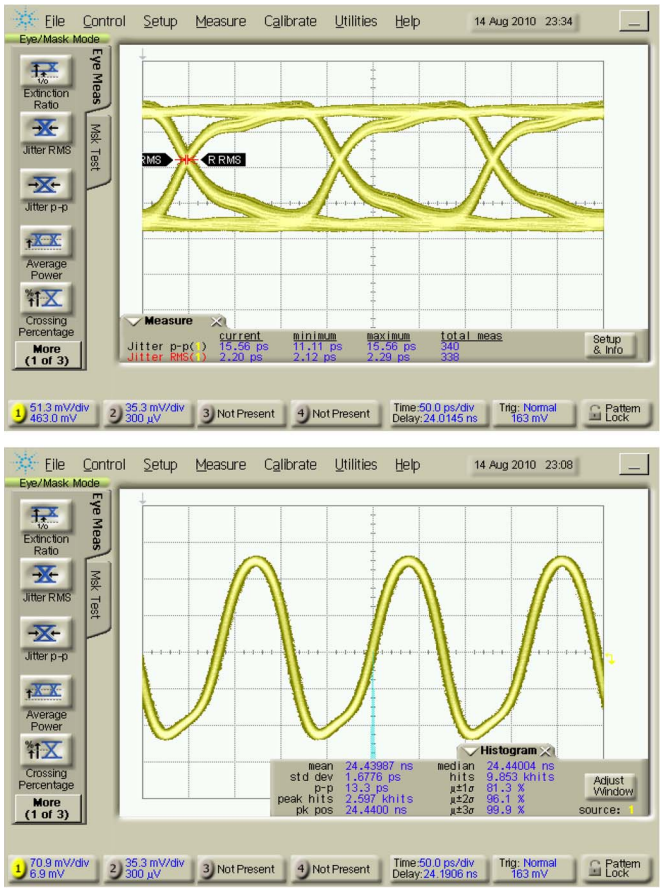

Fig. 9. (a) Measured data eye diagram. (b) Measured recovered clock.

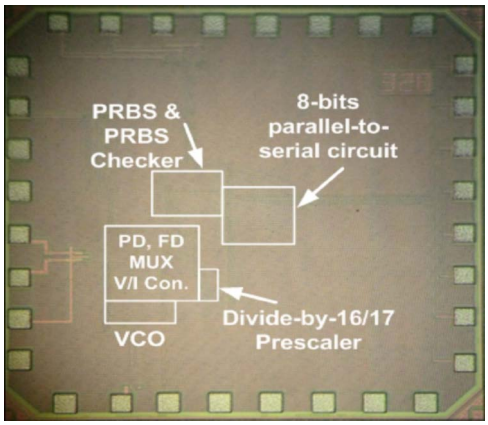

Fig. 10. Die photo.

an FPGA, the on-chip jitter tolerance is measured without external jitter tolerance testing equipment. Due to its digital feature, this technique does not need calibration. This technique can be applied to various analog/digital CDR circuits. Compared with an analog approach in [6], this technique realizes an all-digital approach for the on-chip jitter tolerance measurement. This CDR circuit and the on-chip jitter tolerance measurement can be applied to a 6-Gbps Series-ATA [10] application.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[2]	[6]
Technology	90nm CMOS	40nm CMOS	65nm CMOS
Data rate	6Gb/s	6.375Gb/s	10.2Gb/s ~12.5Gb/s
CDR type	Binary PD	Binary PD	Linear PD
Clock p2p Jitter	13.3ps	N/A	N/A
Data p2p Jitter	15.56ps	39.6ps	N/A
Self-tested Circuit Implementation	All Digital	No	Analog
Calibration	No	No	Yes
Modulation frequency range	178kHz~ 11.3MHz	1MHz~50MHz (by Equipments)	340kHz~ 104MHz
Measured rms error	< 13%	10.4%	< 10%
Area	0.054 mm^2	N/A	0.580 mm^2
Power	44.4mW	N/A	N/A

This technique adopts the sigma–delta approach, and it has a lower data rate under the jitter tolerance measurement compared with a conventional CDR circuit. Although the input data is lowered in this technique, the bandwidth of the CDR circuit is kept constant by scaling the V/I converter by N times. The jitter tolerance is sensitive to the bandwidth, but it is insensitive to the operation frequency of a CDR circuit theoretically. Thus, this technique is useful for CDR circuits.

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